Customer No.: 31561
Docket No.: 10217-US-PA
Application No.: 10/707,608

REMARKS

Present Status of the Application

The Office Action stated to an English language translation of the foreign priority (Taiwan 91137270, filed 12/25/2002) is requested.

The Office Action rejected claims 1-22. Specifically, the Office Action rejected claims 1-22 under 35 U.S.C. 102(b), as being anticipated by Asano (US 2002/0190924).

In response to, Applicant provides an English language translation of the foreign priority (Taiwan 91137270, filed 12/25/2002).

In addition, Applicant has canceled claims 1-11 and 18-20. Applicant has also newly added claims 23-24. The limitation added in claims 23 and 24 is shown in Fig. 4, and no new matter is entered. After entering the amendment, claims 12-17 and 21-24 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicant respectfully traverses the 102(e) rejection of claims 12-22 because Asano (US 2002/0190924) does not teach every element recited in these claims.

> In order to properly anticipate Applicant's claimed invention under 35 U.S.C 102, each and every element of claim in issue must be found, "either expressly or inherently described, in a single prior art reference". "The identical invention must be shown in as complete details as is contained in the claim. Richardson v. Suzuki Motor Co., 868 F. 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. 2131, 8th ed., 2001.

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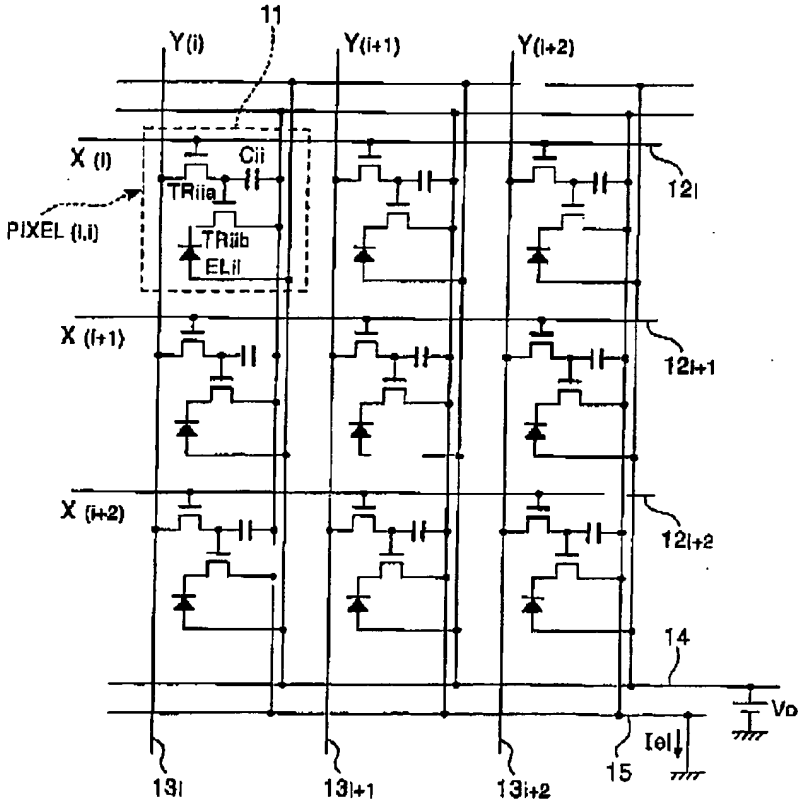
The present invention is in general related to an organic light-emitting display as claim 12 recites:

Claim 12. An organic light-emitting display, comprising:
a pixel array having a plurality of data lines, a plurality of scan lines and a plurality of first and second pixels, wherein each of the first and second pixels is electrically connected to one of the scan lines and one of the data lines correspondingly;
a first external power line, dividing into a plurality of first internal power lines, wherein each first internal power line is electrically connected to at least two of the first pixels;
a second external power line, dividing into a plurality of second internal power lines, wherein each second internal power line is electrically connected to at least two of the second pixels, and the first internal power lines and the second internal power lines are separated; and
a power source electrically connected to the first and second external power lines.

Asano fails to teach or suggest the display includes a first external power line, dividing into a plurality of first internal power lines, wherein each first internal power line is electrically connected to at least two of the first pixels; and a second external power line, dividing into a plurality of second internal power lines, wherein each second internal power line is electrically connected to at least two of the second pixels. The Office Action stated the common power line 14 is as the first external power line of the present invention, and Asano also disclosed the first external power line is divided into a plurality of first internal power lines (connected to Elii). The Office Action also stated the common ground line 15 is as the second external power line of the present invention. However, the common power line 14 and the common ground line 15 are connected to all of the pixels. As Fig. 1 of the Asano reference shown, the common power line 14 is

connected to ELii of the pixel circuit 11 and the common ground line 15 is connected to Cii and TRiib of the pixel circuit 11. That is, the common power line 14 and the common ground line 15 are both connected to ***the same pixel circuit 11***. Asano also teaches the display area of the active matrix display comprises many pixel circuits arranged in a matrix (see paragraph [0023]) and all of the pixel circuits 11 have the same configuration (see paragraph [0024]).



In claim 12 of the present invention, the first external power line is divided into a plurality of first internal power lines, and ***each first internal power line*** electrically connected to at least two of ***the first pixels***; and the second external power line is dividing into a plurality of second internal power lines, and ***each second internal power line*** is electrically connected to at least two of ***the second pixels***. In other words, the first internal power line is electrically connected to a portion of the pixels (first pixels) while the second internal power line is electrically connected to another portion of the pixels (second pixels). The first internal power line and the second internal power line are not electrically connected to the same pixel.

In addition, in the Asano reference, the common power line 14 is connected to Vo while the common ground line 15 is grounded. That is, the common power line 14 and the common ground line 15 are connected to different sources. However, in claim 12 of the present invention, the first and second external power lines are electrically to the same power source.

Therefore, Asano does not teach every element recited in claim 12. For at least the foregoing reasons, Applicant respectfully submits that independent claim 12 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 13-17 patently define over the prior art as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claim.

The present invention also provides an organic light-emitting display as claim 21 recites:

Claim 21. An organic light-emitting display, comprising:
a pixel array having a plurality of data lines, a plurality of scan lines and a plurality of first and second pixels arranged in a matrix of columns and rows, wherein each of the first and second pixels is electrically connected to one of the scan lines and one of the data lines correspondingly;
a first external power line, dividing into a plurality of first internal power lines, wherein each first internal power line is electrically connected to the first pixels in the same column or in the same row;
a second external power line, dividing into a plurality of second internal power lines, wherein each second internal power line is electrically connected to the second pixels in the same column or in the same row, wherein the first internal power lines and the second internal power lines are separated; and
a power source electrically connected to the first and second external power lines.

Asano fails to teach or suggest the display includes a first external power line, dividing into a plurality of first internal power lines, wherein each first internal power line is electrically connected to the first pixels in the same column or in the same row and a second external power line, dividing into a plurality of second internal power lines, wherein each second internal power line is electrically connected to the second pixels in the same column or in the same row. As discussed above, in the Asano reference, the line 14 and the line 15 are connected to all of the pixels. As Fig. 1 of the Asano reference shown, the line 14 is connected to ELii of the pixel circuit 11 and the line 15 is connected to Cii and TRiib of the pixel circuit 11. That is, the line 14 and the line are both connected to ***the same pixel circuit 11.*** However, in claim 21 of the present application, the first external power line is divided into a plurality of first internal power

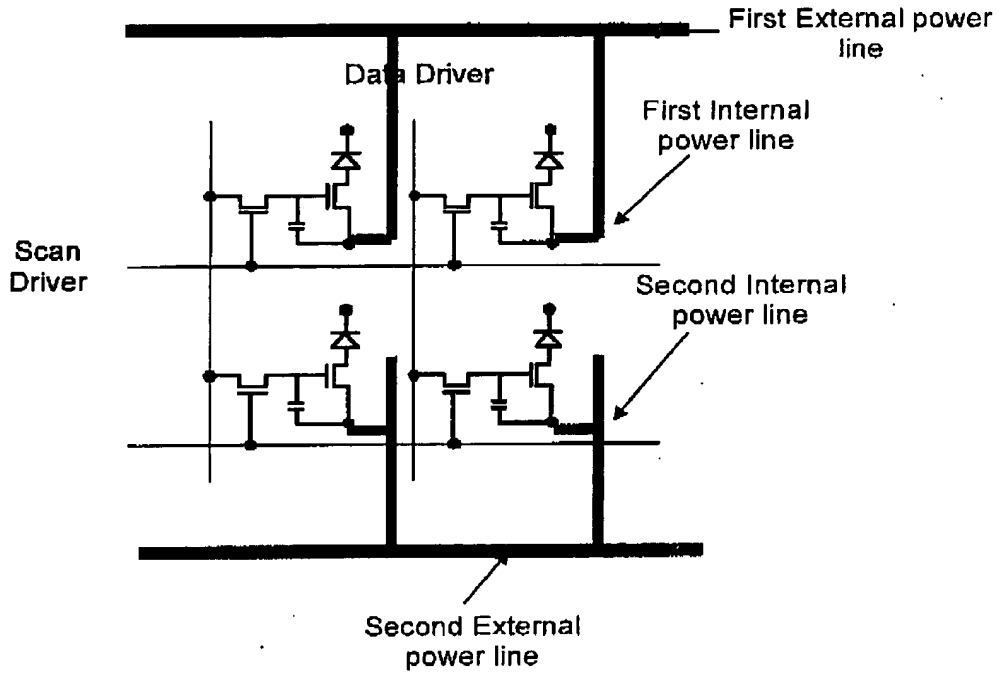
lines, and ***each first internal power line*** electrically connected to at least two of ***the first pixels*** in the same column or in the same row; and the second external power line is dividing into a plurality of second internal power lines, and ***each second internal power line*** is electrically connected to at least two of ***the second pixels*** in the same column or in the same row. In other words, the first internal power line is electrically connected to a portion of the pixels (first pixels) in the same column or in the same row while the second internal power line is electrically connected to another portion of the pixels (second pixels) in the same column or in the same row. The first internal power line and the second internal power line are not electrically connected to the same pixel.

In addition, in the Asano reference, the common power line 14 is connected to Vo while the common ground line 15 is grounded. That is, the common power line 14 and the common ground line 15 are connected to different sources. However, in claim 12 of the present invention, the first and second external power lines are electrically to the same power source.

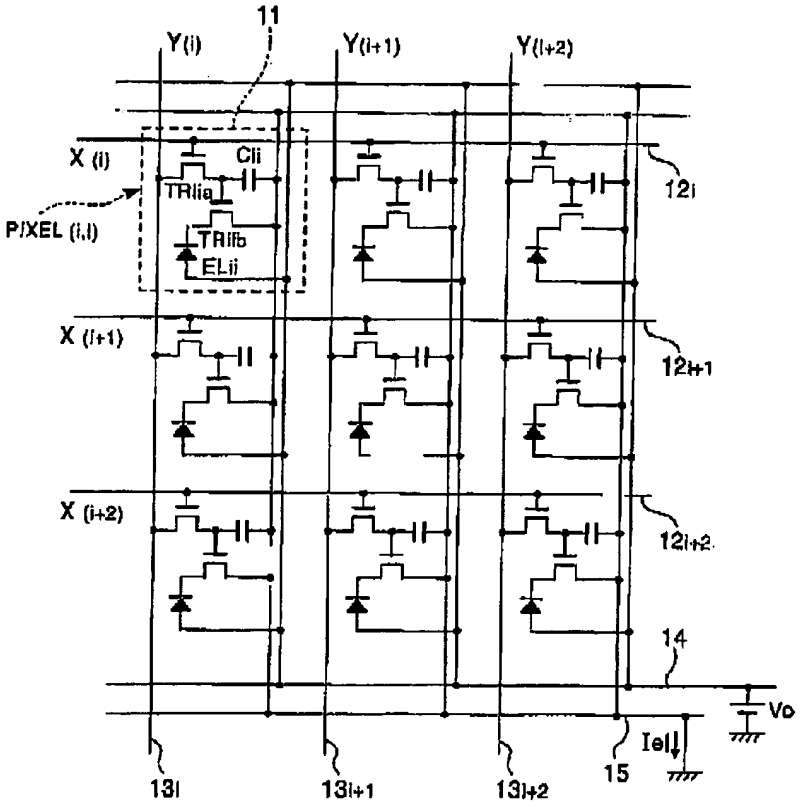
For at least the foregoing reasons, Applicant respectfully submits that independent claim 21 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claim 22 patently define over the prior art as a matter of law.

Newly added claims 23-24

Applicant has newly added claims 23-24, in which the limitation is the first external power line and the second external power line are respectively disposed at two opposite sides of the pixel array, wherein the first internal power lines extend into the pixel array from the external first power line, the second internal power lines extend into the pixel array from the external second power line, and the first internal power lines and the second internal power lines arranged in the same column or in the same row do not extend crossing the whole pixel array. That is as shown in the following drawing.



However, in Fig. 1 of the citation, both the line 14 and the line 15 in the same column or in the same row extend from one side of the array to another side of the array. That is, the line 14 and the line 15 extend crossing the whole pixel array.



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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date : Sept. 1, 2006

Respectfully submitted,

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